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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,749	03/06/2002	Morena Ferrario	Q68642	5241

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EXAMINER	
PANWALKAR, VINEETA S	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,749	FERRARIO ET AL.	
	Examiner	Art Unit	
	Vineeta S. Panwalkar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 March 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Drawings are objected to as to minor informalities.

   - In claims 2 and 5, a method and means respectively, for multiplying the average power values by respective positive constants, wherein the comparison means perform the comparison between the average power values and the products of the average powers by respective positive constants. However, Fig.3 does not disclose the same information and is therefore objected to.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

   Claims 1-3 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, the applicant is claiming a method for selecting the clock signal in a baseband combiner of a space-diversity receiver. However, the applicant is claiming the apparatus ("said combiner comprising: an input for main signal; at least one additional input for a diversity signal; an equalizer receiving at its input said main signal, filtered and sampled and outputting a corresponding equalized main signal; at least one additional corresponding equalizer receiving at its input said at least one diversity signal, filtered and sampled; and outputting a corresponding equalized diversity signal; and a clock recovery circuit") along with the method. Such a claim is rejectable under 35 U.S.C. 112, second paragraph.

Claims 2 and 3 depend on claim 1 and are hence rejected as being dependent on an indefinite claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Monsen (US 3879664), hereafter referred to as Monsen, in view of Nagashima (US 5898741), hereafter referred to as Nagashima.

Regarding claim 1, Monsen discloses a high speed communication receiver comprising:

- An input for a main signal; at least one additional input for a diversity signal; (Receiver lines 11 in Figure 1 and column 4, lines 24-29).
- An equalizer receiving at its input said main signal, filtered and sampled, and outputting a corresponding equalized main signal', at least one corresponding additional equalizer receiving at its input said at least one diversity signal, filtered and sampled, and outputting a corresponding equalized diversity signal (Units 13 in Figure 1 and column 4, line 60 to column 5, line 4. Even though the filter and sampler are not explicitly shown, it is known to people of ordinary skill in the art that the further signal processing is done in digital and hence the filter and sampler are inherent in the system).
- And a clock recovery circuit that is being driven by one of the main signals, filtered and sampled, and at least one of the diversity signals, filtered and sampled. (Figure 9 and column 10, line 56 to column11, line 31).
- A method for selecting the clock signal in a baseband combiner of a space-diversity receiver; the step of driving the clock recovery circuit

by means of one of the main signal, filtered and sampled, and said at least one diversity signal, filtered and sampled. (Figure 1, column 4 line 24- column 5, line 4 and Figure 9, column 10 line 56 to column11, line 31).

Monsen is silent regarding the method for calculating average power.

In the same filed of endeavor, however, Nagashima discloses a delayed detection diversity circuit, comprising:

- The step of driving said clock recovery circuit by means of either one or the other signal, which in turn comprises the steps of: calculating the average power of the equalized main signal and the average power of the at least one equalized diversity signal, and driving the clock recovery circuit by means of the sampled signal chosen on the basis of a comparison between the average power of the main and diversity equalized signals. (Figure 3, where the Received Signal Strength Indicator (RSSI) gives an indication of the average power of each signal. See column 3, lines 15-48).

Therefore it would be obvious to a person of ordinary skill in the art to use average power calculation for the clock recovery, as Nagashima's teachings suggest that synchronization is ensured when a diversity circuit comprises means for detecting a reception branch with maximum RSSI. (Column 2, lines 34- 41). One would be motivated to use the signal with the highest average power because of its high detectability.

Regarding claim 2, Monsen discloses all the subject matter claimed (See above), but is silent about the means for calculating average power and its details. As shown above, Nagashima discloses those means, further comprising:

- Providing a main positive constant and multiplying the main positive constant by the average power of the equalized main signal; and in the instance where at the preceding time of processing the clock recovery circuit driving signal was the main signal, possibly filtered and sampled, driving the clock recovery circuit by means of said at least one diversity signal, possibly filtered and sampled, if and only if the average power of the at least one equalized diversity signal is greater than the product of the main positive constant by the average power of the equalized main signal. (The positive constant is assumed to be one and hence Figure 3 and column 3, lines 15-48 read on claim 2).

Therefore it would be obvious to a person of ordinary skill in the art to use average power calculation for the clock recovery, as Nagashima's teachings suggest that synchronization is ensured when a diversity circuit comprises means for detecting a reception branch with maximum RSSI. (Column 2, lines 34- 41). One would be motivated to use the signal with the highest average power because of its high detectability.

Regarding claim 3, Monsen discloses all the subject matter claimed (See above), but is silent regarding the means for calculating average power and its details.

In the same filed of endeavor, however, Nagashima discloses a delayed detection diversity circuit, comprising the steps of:

- Providing for a diversity positive constant; multiplying the diversity positive constant by the average power of the equalized diversity signal; and, in the instance where at the preceding time processing, the signal that was driving the clock recovery circuit was the diversity signal, possibly filtered and sampled, driving the clock recovery circuit by means of at least one the main signals, possibly filtered and sampled, if and only if the average power of at least one of the equalized main signal is greater than the product of the diversity positive constant by the average power of the equalized diversity signal. (The positive constant is assumed to be one and hence Figure 3 and column 3, lines 15-48 read on claim 2).

Therefore it would be obvious to a person of ordinary skill in the art to use average power calculation for the clock recovery, as Nagashima's teachings suggest that synchronization is ensured when a diversity circuit comprises means for detecting a reception branch with maximum RSSI. (Column 2, lines 34- 41). One would be motivated to use the signal with the highest average power because of its high detectability.

Regarding claim 4, Monsen discloses a high speed communication receiver comprising:

- An input for a main signal; at least one additional input for a diversity signal; (Receiver lines 11 in Figure 1 and column 4, lines 24-29).
- An equalizer receiving at its input said main signal, filtered and sampled, and outputting a corresponding equalized main signal', at least one corresponding additional equalizer receiving at its input said at least one diversity signal, filtered and sampled, and outputting a corresponding equalized diversity signal (Units 13 in Figure 1 and column 4, line 60 to column 5, line 4. Even though the filter and sampler are not explicitly shown, it is known to people of ordinary skill in the art that the further signal processing is done in digital and hence the filter and sampler are inherent in the system).
- And a clock recovery circuit that is being driven by one of the main signals, filtered and sampled, and at least one of the diversity signals, filtered and sampled. (Figure 9 and column 10, line 56 to column11, line 31).

Monsen is silent regarding the means for calculating average power and its details.

In the same filed of endeavor, however, Nagashima discloses a delayed detection diversity circuit, comprising:

- Means for calculating the average power of the main signal and the average power of the at least one diversity signal, means for performing the comparison between the average power values, the clock recovery circuit being driven by means of the sampled signal chosen on the basis of a comparison between the average power of the signals. (Figure 3, where the Received Signal Strength Indicator (RSSI) gives an indication of the average power of each signal. See column 3, lines 15-48).

Therefore it would be obvious to a person of ordinary skill in the art to use average power calculation for the clock recovery, as Nagashima's teachings suggest that synchronization is ensured when a diversity circuit comprises means for detecting a reception branch with maximum RSSI. (Column 2, lines 34- 41). One would be motivated to use the signal with the highest average power because of its high detectability.

Regarding claim 5, Monsen discloses all the subject matter claimed (See above), but is silent regarding the means for calculating average power and its details. As shown above, Nagashima discloses those means, further comprising:

- Means for multiplying the average power values by respective positive constants and wherein the comparison means perform the comparison between the average power values and the products of the average

powers by respective positive constants. (The respective positive constants are assumed to be one and hence Figure 3 and column 3, lines 15-48 read on claim 5).

Therefore it would be obvious to a person of ordinary skill in the art to use average power calculation for the clock recovery, as Nagashima's teachings suggest that synchronization is ensured when a diversity circuit comprises means for detecting a reception branch with maximum RSSI. (Column 2, lines 34- 41). One would be motivated to use the signal with the highest average power because of its high detectability.

Regarding claim 6, Monsen discloses all the subject matter claimed (See above), but is silent regarding the selection means.

In the same filed of endeavor, however, Nagashima discloses a delayed detection diversity circuit, comprising:

- A selection means for selecting the driving signal according to the result of the comparison performed by the comparison means. (Unit 6 in Figure 3 and column 3, lines 15-48).

Therefore it would be obvious to a person of ordinary skill in the art to use average power calculation for the clock recovery, as Nagashima's teachings suggest that synchronization is ensured when a diversity circuit comprises means for detecting a reception branch with maximum RSSI.

(Column 2, lines 34- 41). One would be motivated to use the signal with the highest average power because of its high detectability.

Other Prior Art Cited

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Kazecki et al. (US 5488638) disclose a clock recovery method and apparatus in a diversity receiver.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vineeta S. Panwalkar whose telephone number is 571-272-8561. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

V.P.

JAY K. PATEL
SUPERVISORY PATENT EXAMINER